CLAIMS

Having thus described the invention, what is claimed as new and desirable to be secured by Letters Patent is as follows:

1. A method for fabricating a silicon based package (SBP) comprising:

start with a wafer composed of silicon and having a first surface and a reverse surface which are planar as the base for the SBP,

forming an interconnection structure including multilayer conductor patterns over the first surface,

forming a temporary bond between the SBP and a wafer holder, with the wafer holder being a rigid structure,

thinning the wafer to a desired thickness to form an ultra thin silicon wafer (UTSW) for the SBP,

forming via holes which extend through the UTSW, and

forming metallization in the via holes with the metallization extending through the UTSW.

2. The method of claim 1 including bonding the metallization in the via holes to pads of a carrier.

3. The method of claim 1 including forming capture pads on the first surface prior to thinning the wafer.

4. The method of claim 1 including:

initially forming capture pads on the first surface,

then forming the interconnection structure over the first surface and the capture pads,

then forming the temporary bond of the wafer holder to the reverse surface, and

then thinning the wafer, thereby forming the UTSW.

5. The method of claim 1 including:

initially forming capture pads on the first surface,

then forming interconnection structure over the first surface and the capture pads,

then forming the temporary bond of the wafer holder to the reverse surface,

then thinning the wafer, thereby forming the UTSW, and

then forming the via holes through the UTSW down to the capture pads.

6. The method of claim 1 including:

initially forming capture pads on the first surface,

then forming interconnection structure over the first surface and the capture pads,

then forming the temporary bond of the wafer holder to the reverse surface,

then thinning the wafer, thereby forming the UTSW,

then forming the via holes through the UTSW down to the capture pads,

then forming a dielectric layer over the surface of the wafer leaving the bottoms of the via holes clear with the capture pads exposed, and

then forming the metallization in the via holes in contact with the capture pads.

7. The method of claim 1 including:

initially forming capture pads on the first surface,

then forming interconnection structure over the first surface and the capture pads

then forming the temporary bond of the wafer holder to the reverse surface,

then thinning the wafer, thereby forming the UTSW,

then forming the via holes through the UTSW down to the capture pads,

then forming a dielectric layer over the surface of the wafer leaving the bottoms of the via holes clear with the capture pads exposed,

then depositing metal pads into the via holes in contact with the capture pads, and

then form metal joining structures on the metal pads.

8. The method of claim 1 including initially forming via holes in the first surface prior to thinning the wafer.

9. The method of claim 1 including the steps as follows:

initially forming via holes in the first surface prior to thinning the wafer,

then forming a dielectric layer covering the via holes.

10. The method of claim 1 including the steps as follows:

initially forming via holes in the first surface prior to thinning the wafer,

then forming a dielectric layer over the surface of the wafer including the via holes, and

then forming a through via/cap pad layer of a first metal layer over dielectric layer including the via holes.

11. The method of claim 1 including the steps as follows:

initially forming via holes in the first surface prior to thinning the wafer,

then forming a dielectric layer over the surface of the wafer including the via holes,

then forming a through via/cap pad layer of a first metal layer over dielectric layer including the via holes, and

then planarizing to remove the via/cap pad layer above the surface of the dielectric layer, thereby forming vias in the via holes.

12. The method of claim 1 including the steps as follows:

initially forming via holes in the first surface prior to thinning the wafer,

then forming a dielectric layer over the surface of the wafer including the via holes,

then forming a through via/cap pad layer of a first metal layer over dielectric layer including the via holes,

then planarizing to remove the via/cap pad layer above the surface of the dielectric layer, thereby forming vias in the via holes, and

then forming an interconnection structure over the first surface including the first metal layer.

13. The method of claim 1 including the steps as follows:

initially forming via holes in the first surface prior to thinning the wafer,

then forming a dielectric layer over the surface of the wafer including the via holes,

then forming a through via/cap pad layer of a first metal layer over dielectric layer including the via holes,

then planarizing to remove the via/cap pad layer above the surface of the dielectric layer, thereby forming vias in the via holes, and

then forming interconnection structure over the first surface including the metal vias and the first metal layer,

then forming the temporary bond to the rigid wafer holder on the reverse surface, and

then thinning the wafer to the desired thickness of the UTSW.

14. A method for fabricating a silicon based package (SBP) comprising:

providing a base for the SBP comprising a wafer composed of silicon and having a first surface and a reverse surface which are planar,

forming via holes which extend partially through the wafer from the first surface towards the reverse surface with the each via hole having a base thereof which is closest to the reverse surface,

forming a dielectric layer covering the first surface of the silicon wafer and the via holes with distal portions of the dielectric layer being located at the bases of the via holes, so that the distal portions are closest to the reverse surface,

forming metal vias in the via holes on the dielectric layer with proximal ends being located at the first surface and distal ends of the metal vias being located on the distal portions of the dielectric layer, thereby being closest to the reverse surface,

forming an interconnection structure including multilayer conductor patterns over the metal vias and the dielectric layer,

forming a temporary bond between the SBP and a wafer holder, with the wafer holder being a rigid structure leaving the reverse surface of the wafer exposed,

thinning the wafer to a desired thickness to form an ultra thin silicon wafer (UTSW) for the SBP exposing the distal portions of the dielectric layer covering the distal ends of the metal vias, and

removing the distal portions of the dielectric layer exposing the distal ends of the metal vias which extend through the UTSW.

SUB A2 Cont.

15. The method of claim 14 including the steps of forming the metal vias by forming a blanket through via/cap pad layer of a first metal layer over dielectric layer including the via holes, followed by planarizing the via/cap pad layer down to the surface of the dielectric layer, thereby forming the metal vias in the via holes.

16. The method of claim 14 including the steps of forming the metal vias by forming a blanket through via/cap pad layer of a first metal layer over dielectric layer including the via holes, followed by planarizing to remove the via/cap pad layer above the surface of the dielectric layer, thereby forming the metal vias in the via holes,

then forming the interconnection structure over the first surface including the metal vias and the first metal layer,

then forming the temporary bond to a rigid wafer holder on the reverse surface, and

then thinning the wafer to the desired thickness of the UTSW.

17. A silicon based package (SBP) comprising:

an ultra thin silicon wafer (UTSW) composed of silicon and having a first surface and a reverse surface,

capture pads formed on the first surface,

an interconnection structure formed over the first surface and the capture pads,

via holes formed in the SBP which extend from the reverse surface through the UTSW to the capture pads, and

metal vias formed in the via holes which extend through the UTSW.

18. The silicon based package (SBP) of claim 17 with the metal vias being bonded to pads of a carrier.

19. The silicon based package (SBP) of claim 17 comprising the interconnection structure including bonds formed to connectors of semiconductor chips.

20. The silicon based package (SBP) of claim 17 comprising the interconnection structure including bonds formed to C4 solder ball connectors of semiconductor chips.

21. A silicon based package (SBP) comprising:

an ultra thin silicon wafer (UTSW) composed of silicon and having a first surface and a reverse surface,

via holes formed in the UTSW which extend from the reverse surface through the UTSW to the first surface, the via holes having sidewalls and bottoms,

a dielectric layer formed covering the first surface and the sidewalls and bottoms of the via holes,

metal vias formed on the dielectric layer in the via holes and extending through the UTSW to the reverse surface,

an interconnection structure formed over the first surface and the metal vias, and

the metal vias being bonded to pads of a carrier.

22. The silicon based package (SBP) of claim 21 with the metal vias being bonded to pads of a carrier.

23. The silicon based package (SBP) of claim 21 comprising the interconnection structure including bonds formed to connectors of semiconductor chips.

24. The silicon based package (SBP) of claim 21 comprising the interconnection structure including bonds formed to C4 solder ball connectors of semiconductor chips.